

8-bit high-speed analog-to-digital converter

TDA8703/8703T

FEATURES

- 8-bit resolution
- Sampling rate up to 40 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.1 effective bits at 4.43 MHz full-scale input)
- Binary or two's complement 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Internal reference voltage generator
- Power dissipation only 290 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

- General purpose high-speed analog-to-digital conversion
- Digital TV, IDTV
- Subscriber TV decoder
- Satellite TV decoders
- Digital VCR

GENERAL DESCRIPTION

The TDA8703 is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are TTL compatible, although a low-level AC clock input signal is allowed.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8703	24	DIL	plastic	SOT101
TDA8703T	24	SO24	plastic	SOT137A

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current		—	28	36	mA
I_{CCD}	digital supply current		—	19	25	mA
I_{CCO}	output stages supply current		—	11	14	mA
ILE	DC integral linearity error		—	—	± 1	LSB
DLE	DC differential linearity error		—	—	$\pm 1/2$	LSB
AILE	AC integral linearity error	note 1	—	—	± 2	LSB
B	-3 dB bandwidth	note 2; $f_{CLK} = 40$ MHz	—	19.5	—	MHz
$f_{CLK}/f_{\overline{CLK}}$	maximum conversion rate	note 3	40	—	—	MHz
P_{tot}	total power dissipation		—	290	415	mW

Notes to the quick reference data

1. Full-scale sinewave ($f_i = 4.4$ MHz; f_{CLK} ; $f_{\overline{CLK}} = 27$ MHz).
2. The -3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at input).
3. The circuit has two clock inputs CLK and \overline{CLK} . There are four modes of operation:
 - TTL (mode 1); \overline{CLK} decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
 - TTL (mode 2); CLK decoupled to DGND by a capacitor. \overline{CLK} input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
 - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the CLK input with such a signal, sampling takes place on the HIGH-to-LOW transition.

If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

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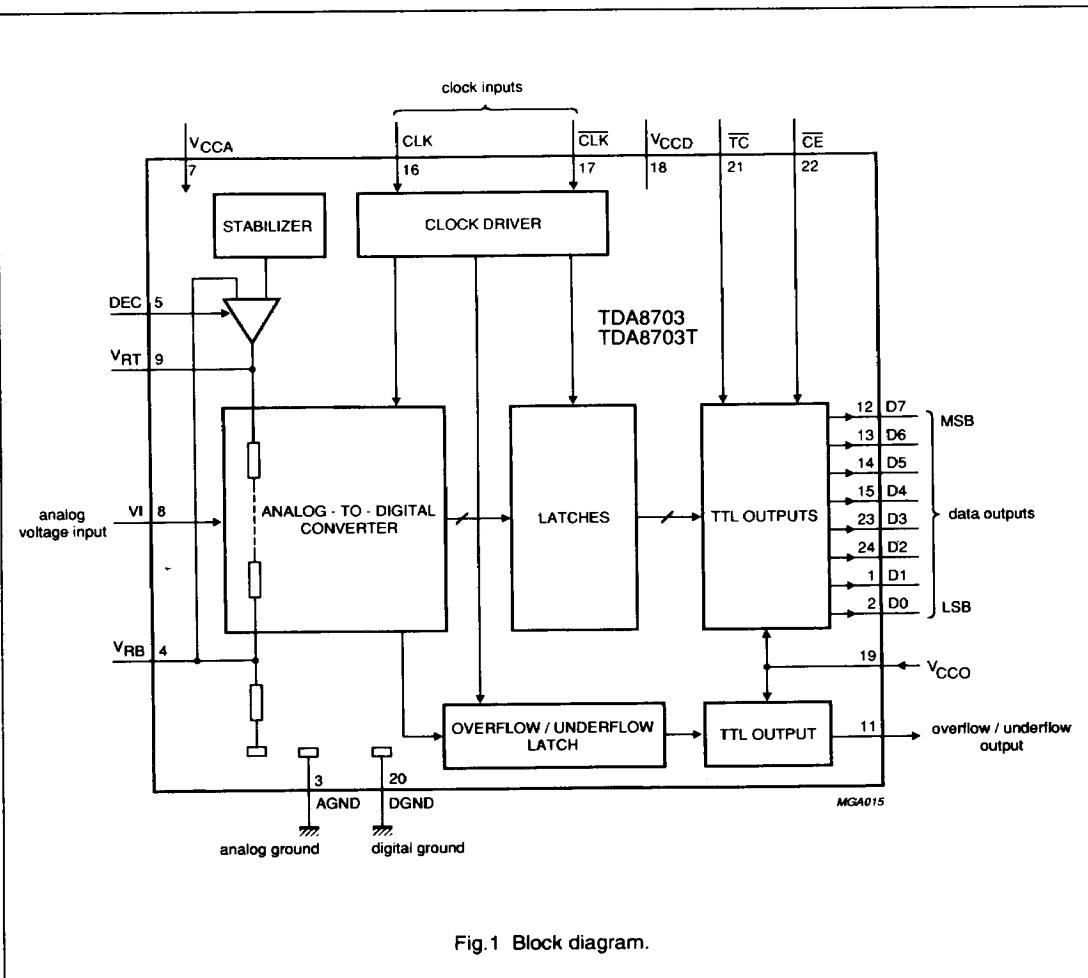
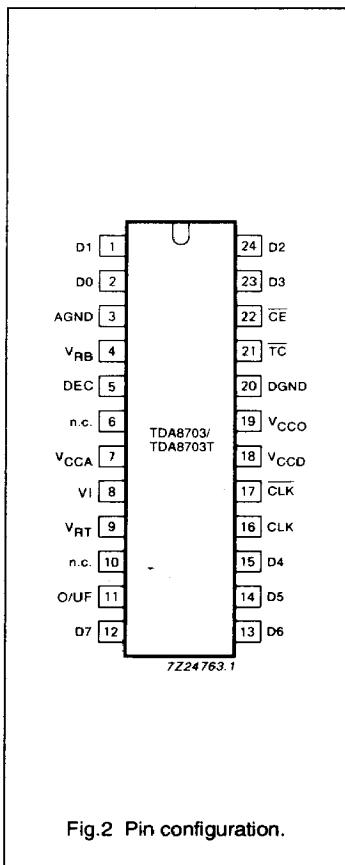


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
AGND	3	analog ground
V _{RB}	4	reference voltage bottom (decoupling)
DEC	5	decoupling input (internal stabilization loop decoupling)
n.c.	6	not connected
V _{CCA}	7	positive supply voltage for analog circuits (+5 V)
VI	8	analog voltage input
V _{RT}	9	reference voltage top (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output, bit 7 (MSB)
D6	13	data output, bit 6
D5	14	data output, bit 5
D4	15	data output, bit 4
CLK	16	clock input
CLK	17	complementary clock input
V _{CCD}	18	positive supply voltage for digital circuits (+5 V)
V _{CCO}	19	positive supply voltage for output stages (+5 V)
DGND	20	digital ground
TC	21	input for two's complement output (TTL level input, active LOW)
CE	22	chip enable input (TTL level input, active LOW)
D3	23	data output, bit 3
D2	24	data output, bit 2

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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range		-0.3	7.0	V
V_{CCD}	digital supply voltage range		-0.3	7.0	V
V_{CCO}	output stages supply voltage		-0.3	7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differences		-1.0	1.0	V
$V_{CCO} - V_{CCD}$	supply voltage differences		-1.0	1.0	V
$V_{CCA} - V_{CCO}$	supply voltage differences		-1.0	1.0	V
V_{VI}	input voltage range	referenced to AGND	-0.3	7.0	V
$V_{CLK(p-p)}/V_{CLK(p-p)}$	AC input voltage for switching (peak-to-peak value)	see note; referenced to DGND	-	2.0	V
I_O	output current		-	+10	mA
T_{STG}	storage temperature range		-55	+150	°C
T_{AMB}	operating ambient temperature range		0	+70	°C
T_j	junction temperature		-	+125	°C

Note to the limiting valuesThe circuit has two clock inputs CLK and \bar{CLK} . There are four modes of operation:

- TTL (mode 1); CLK decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
- TTL (mode 2); CLK decoupled to DGND by a capacitor. \bar{CLK} input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
- AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the \bar{CLK} input with such a signal, sampling takes place on the HIGH-to-LOW transition.

If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th(j-a)}$	from junction to ambient in free air (SOT101)	55 K/W
$R_{th(j-a)}$	from junction to ambient in free air (SOT137A)	75 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

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CHARACTERISTICS (see Tables 1 and 2)

$V_{CCA} = V_7 - V_3 = 4.5 \text{ V to } 5.5 \text{ V}$; $V_{CCD} = V_{18} - V_{20} = 4.5 \text{ V to } 5.5 \text{ V}$; $V_{CCO} = V_{19} - V_{20} = 4.5 \text{ V to } 5.5 \text{ V}$; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5 \text{ V to } +0.5 \text{ V}$; $V_{CCO} - V_{CCD} = -0.5 \text{ V to } +0.5 \text{ V}$; $V_{CCA} - V_{CCO} = -0.5 \text{ V to } +0.5 \text{ V}$; $T_{amb} = 0^\circ\text{C} \text{ to } +70^\circ\text{C}$; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5 \text{ V}$ and $T_{amb} = 25^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current		—	28	36	mA
I_{CCD}	digital supply current		—	19	25	mA
I_{CCO}	output stage supply current	all outputs LOW	—	11	14	mA
Inputs						
CLOCK INPUT CLK AND \bar{CLK} (NOTE 1; REFERENCED TO DGND)						
V_{IL}	LOW level input voltage		0	—	0.8	V
V_{IH}	HIGH level input voltage		2.0	—	V_{CCD}	V
I_{IL}	LOW level input current	$V_{CLK}/V_{\bar{CLK}} = 0.4 \text{ V}$	-400	—	—	μA
I_{IH}	HIGH level input current	$V_{CLK}/V_{\bar{CLK}} = 0.4 \text{ V}$ $V_{CLK}/V_{\bar{CLK}} = V_{CCD}$	—	—	100	μA
—			—	—	300	μA
Z_i	input impedance	$f_{CLK}/f_{\bar{CLK}} = 10 \text{ MHz}$	—	4	—	$\text{k}\Omega$
C_i	input capacitance	$f_{CLK}/f_{\bar{CLK}} = 10 \text{ MHz}$	—	4.5	—	pF
$V_{CLK(p-p)} - V_{\bar{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)	note 1; DC level = 1.5 V	0.5	—	2.0	V
INPUTS $\bar{T}C$ AND \bar{CE} (referenced to DGND)						
V_{IL}	LOW level input voltage		0	—	0.8	V
V_{IH}	HIGH level input voltage		2.0	—	V_{CCD}	V
I_{IL}	LOW level input current	$V_{IL} = 0.4 \text{ V}$	-400	—	—	μA
I_{IH}	HIGH level input current	$V_{IH} = 2.7 \text{ V}$	—	—	20	μA
VI (analog input voltage referenced to AGND)						
$V_{VI(B)}$	input voltage (bottom)		1.33	1.41	1.48	V
$V_{VI(0)}$	input voltage	output code = 0	1.455	1.55	1.635	V
$V_{OS(B)}$	offset voltage (bottom)	$V_{VI(0)} - V_{VI(B)}$	0.125	—	0.155	V
$V_{VI(T)}$	input voltage (top)		3.2	3.36	3.5	V
$V_{VI(255)}$	input voltage	output code = 255	3.115	3.26	3.385	V
$V_{OS(T)}$	offset voltage (top)	$V_{VI(T)} - V_{VI(255)}$	0.085	—	0.115	V
$V_{VI(p-p)}$	input voltage amplitude (peak-to-peak value)		1.66	1.71	1.75	V
I_{IL}	LOW level input current	$V_{VI} = 1.4 \text{ V}$	—	0	—	μA
I_{IH}	HIGH level input current	$V_{VI} = 3.6 \text{ V}$	60	120	180	μA

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CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VI (analog input voltage referenced to AGND)						
Z_i	input impedance	$f_i = 1 \text{ MHz}$	-	10	-	$\text{k}\Omega$
C_i	input capacitance	$f_i = 1 \text{ MHz}$	-	14	-	pF
Reference resistance						
R_{ref}	reference resistance	$V_{\text{RT}} \text{ to } V_{\text{RB}}$	-	220	-	Ω
Outputs						
DIGITAL OUTPUTS (D7 - D0) (REFERENCED TO DGND)						
V_{OL}	LOW level output voltage	$I_o = 1 \text{ mA}$	0	-	0.4	V
V_{OH}	HIGH level output voltage	$I_o = -0.4 \text{ mA}$	2.7	-	V_{CCD}	V
I_{OZ}	output current in 3-state mode	$0.4 \text{ V} < V_o < V_{\text{CCD}}$	-20	-	+20	μA
Switching characteristics (note 2; see Fig.3)						
$f_{\text{CLK}}/\overline{f_{\text{CLK}}}$	maximum clock frequency		40	-	-	MHz
Analog signal processing ($f_{\text{CLK}} = 40 \text{ MHz}$)						
B	-3 dB bandwidth	note 3	-	19.5	-	MHz
G_d	differential gain	note 4	-	0.6	-	%
ϕ_d	differential phase	note 4	-	0.8	-	deg
f_i	fundamental harmonics (full-scale)	$f_i = 4.43 \text{ MHz}$	-	-	0	dB
f_{all}	harmonics (full-scale), all components	$f_i = 4.43 \text{ MHz}$	-	-55	-	dB
SVRR1	supply voltage ripple rejection	note 5	-	-28	-25	dB
SVRR2	supply voltage ripple rejection	note 5	-	1	2.5	%/V
Transfer function						
ILE	DC integral linearity error		-	-	± 1	LSB
DLE	DC differential linearity error		-	-	$\pm 1/2$	LSB
AILE	AC integral linearity error	note 6	-	-	± 2	LSB
eff	effective bits	$f_i = 4.43 \text{ MHz}$	-	7.1	-	bits
Timing (note 7; see Figs 3 to 6; $f_{\text{CLK}} = 40 \text{ MHz}$)						
t_{S}	sampling delay		-	-	2	ns
t_{HD}	output hold time		6	-	-	ns
t_{tLH}	output delay time	LOW-to-HIGH transition	-	8	10	ns
t_{tHL}	output delay time	HIGH-to-LOW transition	-	14	16	ns
t_{tZH}	3-state output delay times	enable-to-HIGH	-	19	25	ns
t_{tZL}	3-state output delay times	enable-to-LOW	-	16	20	ns
t_{tHZ}	3-state output delay times	disable-to-HIGH	-	14	20	ns
t_{tLZ}	3-state output delay times	disable-to-LOW	-	9	12	ns

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Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{\text{CLK}}$. There are four modes of operation:
 - TTL (mode 1); $\overline{\text{CLK}}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
 - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{\text{CLK}}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
 - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{\text{CLK}}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.
- If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.
2. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 2 ns.
 3. The -3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
 4. Low frequency ramp signal ($V_{V_{I(p-p)}} = 1.8$ V and $f_i = 15$ kHz) combined with a sinewave input voltage ($V_{V_{I(p-p)}} = 0.5$ V, $f_i = 4.43$ MHz) at the input.
 5. Supply voltage ripple rejection:
 - SVRR1; variation of the input voltage producing output code 127 for supply voltage variation of 1 V:
 $\text{SVRR1} = 20 \log (\Delta V_{V_{I(127)}} / \Delta V_{\text{CCA}})$
 - SVRR2; relative variation of the full-scale range of analog input for a supply voltage variation of 1 V:
 $\text{SVR2} = \{\Delta(V_{V_{I(0)}} - V_{V_{I(255)}}) / (V_{V_{I(0)}} - V_{V_{I(255)}})\} + \Delta V_{\text{CCA}}$
 6. Full-scale sinewave ($f_i = 4.4$ MHz; $f_{\text{CLK}}, f_{\overline{\text{CLK}}} = 27$ MHz).
 7. Output data acquisition:
 - Output data is available after the maximum delay of $t_{d_{HL}}$ and $t_{d_{LH}}$.
 - Output data is fully stable during the low level of the clock. Thus it is recommended that acquisition of this data is made after the falling edge of the clock, instead of after the maximum ($t_{d_{HL}}, t_{d_{LH}}$).

Table 1 Output coding and input voltage (typical values; referenced to AGND)

STEP	$V_{V_{I(p-p)}}$	O/UF	BINARY OUTPUT BITS								TWO's COMPLEMENT OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow	< 1.55	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1.55	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	-	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
254	•	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	3.26	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow	> 3.26	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

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Table 2 Mode selection

$\overline{\text{TC}}$	$\overline{\text{CE}}$	D7 - D0	O/UF
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

Where: X = don't care

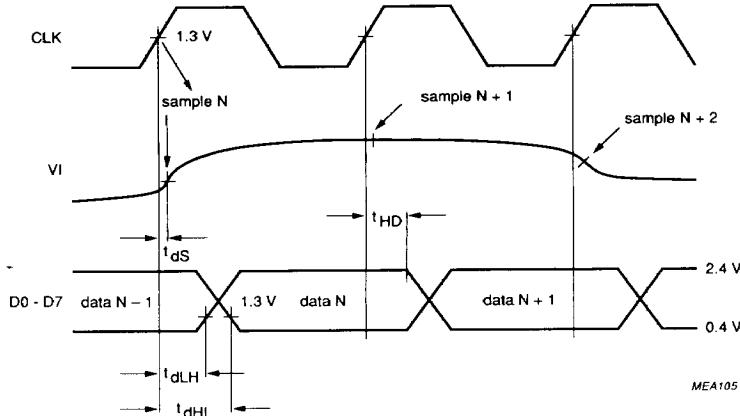


Fig.3 Timing diagram.

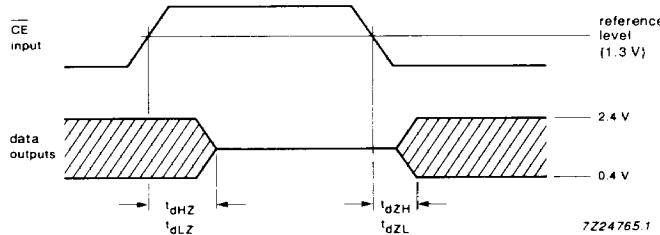
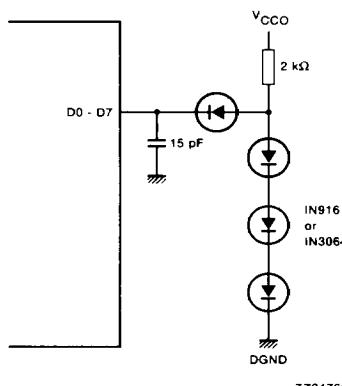
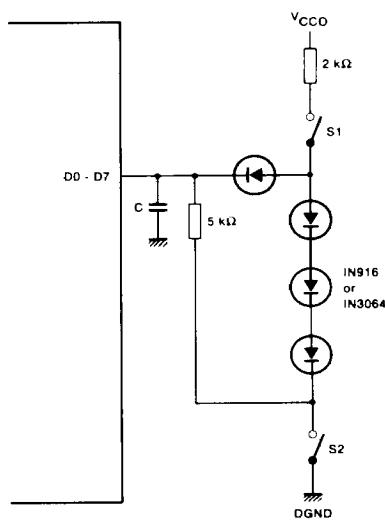


Fig.4 3-state delay timing diagram.

**8-bit high-speed
analog-to-digital converter****TDA8703/8703T**Fig.5 Load circuit for timing measurement; data outputs (\overline{CE} = LOW).Fig.6 Load circuit for timing measurement; 3-state outputs (\overline{CE} : $f_i = 1 \text{ MHz}$; $V_{VI} = 3 \text{ V}$); see Table 3.

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Table 3 Timing measurement for load circuit

TIMING MEASUREMENT	SWITCH S1	SWITCH S2	CAPACITOR
t_{dZH}	open	closed	15 pF
t_{dZL}	closed	open	15 pF
t_{dHZ}	closed	closed	5 pF
t_{dLZ}	closed	closed	5 pF

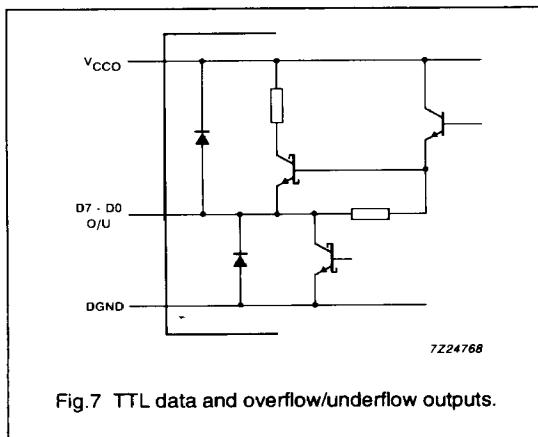
INTERNAL PIN CONFIGURATIONS

Fig.7 TTL data and overflow/underflow outputs.

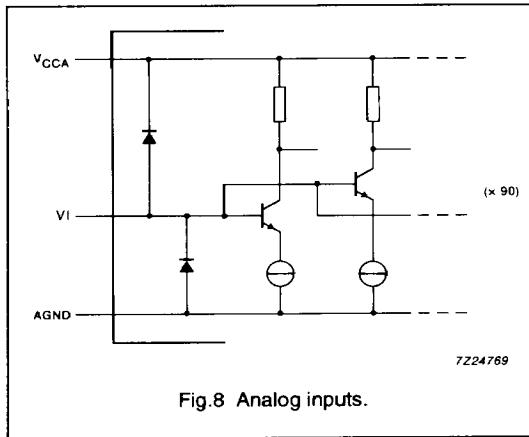


Fig.8 Analog inputs.

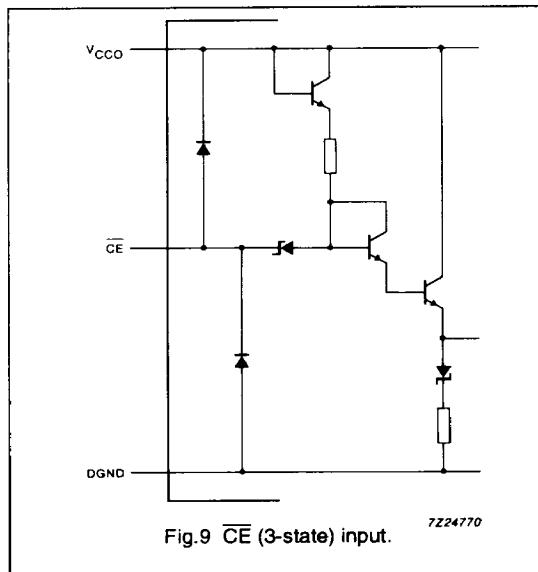


Fig.9 CE (3-state) input.

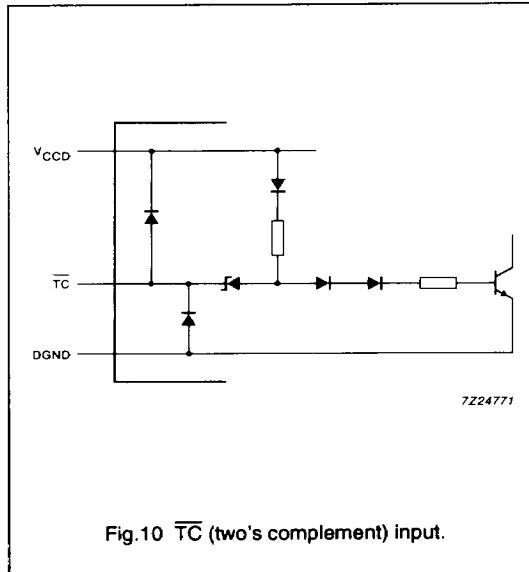
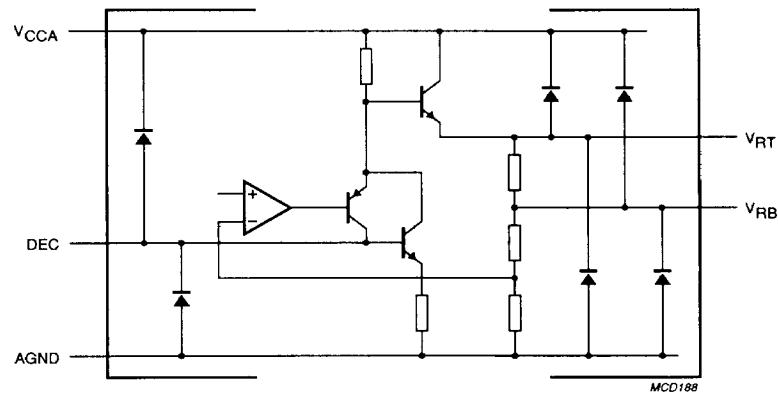
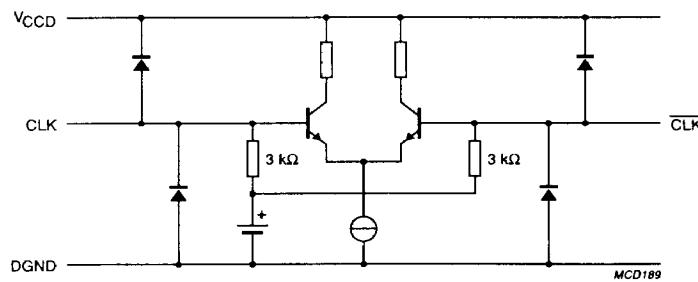


Fig.10 TC (two's complement) input.

**8-bit high-speed
analog-to-digital converter****TDA8703/8703T**Fig.11 V_{RB} , V_{RT} and DEC .Fig.12 CLK and \overline{CLK} inputs.

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APPLICATION INFORMATION

Additional application information
will be supplied upon request
(please quote number FTV/8901).

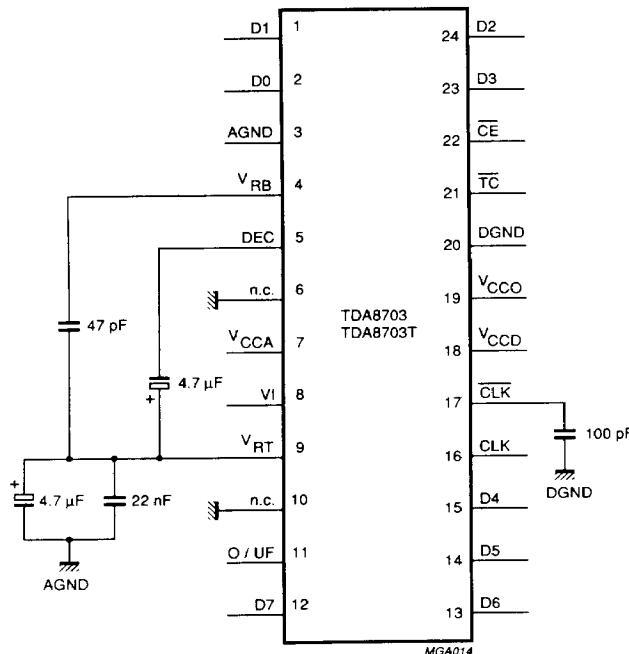


Fig.13 Application diagram.

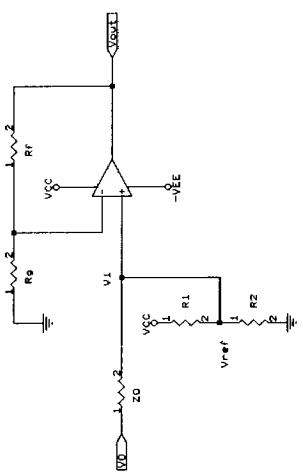
Notes to Fig.13

1. CLK should be decoupled to the DGND with a 100 nF capacitor, if a TTL signal is used on CLK (see 'Notes to the characteristics', note 1).
2. CLK and $\overline{\text{CLK}}$ can be used in a differential mode (see 'Notes to the characteristics', note 1).
3. V_{RB} and V_{RT} are decoupling pins for the internal reference ladder; do not draw current from these pins in order to achieve good linearity.
4. Analog and digital supplies should be separated and decoupled.
5. Pins 6 and 10 should be connected to AGND in order to prevent noise influence.

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DC GAIN AND OFFSET CIRCUIT AND FORMULAS FOR INTERFACING TO TDA8703



INITIAL ASSUMPTIONS:

1. $Z_0 = R_1 / R_2$
2. $V_{ref} = V_{cc} - R_2 / 2 * (R_1 + R_2)$ WHEN $V_0 = 0$
3. VOLTAGE AT $V_1 = V_0 / 2 + V_{ref}$
4. OP AMP GAIN, $A = (R_f + R_g) / R_q$ THIS IS AC COMPONENT + DC COMPONENT
5. $V_0 = A * (V_0 / 2) + A * V_{ref}$ AND THAT $R_1 = R_2 * Z_0 / (R_2 - Z_0)$

IT FOLLOWS THAT $R_2 = (Z_0 * 2 * V_{ref} + Z_0 * (V_{cc} - 2 * V_{ref})) / (V_{cc} - V_2 * V_{ref})$
THE TDA8703 HAS A $V_{in\ (LOW)} = 1.65\text{VDC}$ AND A $V_{in\ (HIGH)} = 3.45\text{VDC}$
THEREFORE THE DC OFFSET IS 1.65VDC AND THE AC SWING IS 1.80VPP
FOR A VIDEO SOURCE, ASSUME $Z_0 = 750\text{ohms}$ AND $V_0 = 1\text{VPP}$, ALSO $V_{cc} = 5\text{VDC}$.

THEREFORE $R_2 = 91.40\text{ohms}$ AND $R_1 = 417.90\text{ohms}$

NOTES:

- OP AMP BANDWIDTH SHOULD BE 50 MHZ OR BETTER
- Z_0 SHOULD BE LOW FOR HIGH FREQUENCY APPLICATIONS
- INCLUDE V_0 SOURCE IMPEDANCE WHEN DETERMINING VALUE OF Z_0

SEGNETICS / PHILIPS COMPONENTS	
Title	B7030FF, SCH
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